EFFECT OF VOLTAGE LEVELS AND MODULATION INDEX ON THD OF A DIODE CLAMPED MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

Y.Krishna Priya * and Dr.M.Vijaya Kumar **

*Assistant Professor, Department of Electrical and Electronics Engineering,
Intell Engineering College; Ananthapur; A.P, India.
**Professor, Department of Electrical & Electronics Engineering,
JNTUA Ananthapur, A.P, India.

ABSTRACT: The advantage of AC drive over DC drive is rugged construction and low cost. Due to this reason most of the industrial applications uses induction motor drive. For the speed control of induction motor drive we need inverter. Conventionally three level sinusoidal pulse width modulated (SPWM) inverters are popular for this application. But the drawback of three level SPWM inverters is high switching losses due to high switching frequency. So conventional inverters are limited for low power applications only. For medium and high power application multilevel inverters (MLI) are proposed in literature. Out of various configurations of MLI Dioide clamped MLI is popular. It has the advantages of simple configuration and requires less number of individual DC sources. In this paper we have considered 3 Level, 5 Level and 7 Level MLI fed induction motor drive. We have done the analyses of effect of voltage levels and modulation index on total harmonic distortion (THD). A Simulink based model is developed and simulation results are presented for various test cases. It is clearly shown that as we increase the voltage levels and modulation index THD is reducing. The maximum levels of the inverter limited to seven based on cost factor of the drive.

KEYWORDS: SPWM, Voltage levels, THD, Induction motor drive.

INTRODUCTION

In recent years the industrial demand increases to high power equipments up to mega watts level. But the power handling capacity of power semiconductor devices are less only up to kilo volts level. The controlled ac drives in that range are connected with medium voltage networks. To increase the power handling capacity, multilevel topologies are proposed since 1980s. A 3-level inverter generates an output voltage with two values and 5-level and 7-level inverter generates an output voltage of three values and so on. Increasing the number of levels increases the number of steps in the output. The advantages of multilevel topologies are, the voltage across each power semiconductor devices are less, the output voltage harmonic distortion are reduced [1, 2]. However the drawbacks are, the required number of power semiconductor devices are increased and control becomes more complex [1, 2]. They can also used for medium or even low power application with better performance [3].

The main topologies of multilevel inverters are diode clamped or neutral point clamped multilevel inverter (DCMLI), capacitor clamped or flying capacitor multilevel inverter (FCMLI) and cascaded H-bridge multilevel inverter (CHBMLI). Comparing the devices and components used, the diode clamped inverter requires more number of diodes and the flying capacitor inverter requires more number of capacitors while the cascaded H-bridge inverter requires less number [4].

DIODE-CLAMPED MULTILEVEL INVERTER

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is

to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is Vdc. An n level inverter needs (n-1) voltage sources, 2(n-1) switching devices and (n-1) (n-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform.

A.3-LEVEL DIODE CLAMPED INVERTER

The three phase 3-level diode clamped multilevel inverter fed induction motor is the common multilevel inverter used for various applications [8]. A three phase 3-level diode clamped multilevel inverter is adopted in this paper. It is obtained from a configuration of twelve switching devices and six clamping diodes as shown in figure.1.

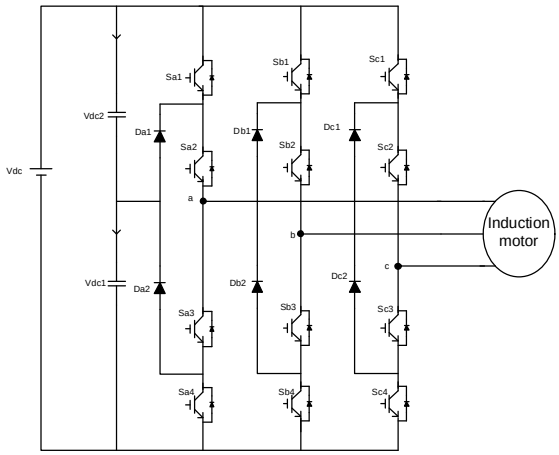

Figure 1. Diode-Clamped Multilevel Inverter Circuit Topologies for three phase three-level fed induction motor

The sector is identified from three phase reference voltage and the corresponding voltage vector is selected from the switching table to generate the gating pulses for the inverter.

Table1. Three-level diode clamped switching sate for phase A

	Sa1	Sa2	Sa3	Sa4
Vdc/2	1	1	0	0
0	0	1	1	0
-Vdc/2	0	0	1	1

B.5-LEVEL DIODE CLAMPED INVERTER

The three phase 5-level diode clamped multilevel inverter fed induction motor is the common multilevel inverter used for various applications. A three phase 5-level diode clamped multilevel inverter is adopted in this paper. It is obtained from a configuration of 24 switching devices and 18 clamping diodes as shown in figure.

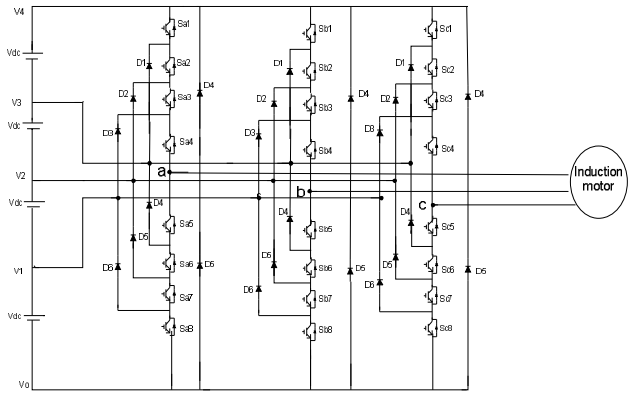

Figure 2. Diode-Clamped Multilevel Inverter Circuit Topologies for three phase Five-level fed induction motor

The sector is identified from three phase reference voltage and the corresponding voltage vector is selected from the switching table to generate the gating pulses for the inverter.

Table 2. Five-level diode clamped switching sate for phase A

V0	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Sa7	Sa8
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
Vdc/4	0	0	0	1	1	1	1	0
Vdc/2	0	0	0	0	1	1	1	1

C.7-LEVEL DIODE CLAMPED INVERTER

The three phase 7-level diode clamped multilevel inverter fed induction motor is the common multilevel inverter used for various applications. A three phase 7-level diode clamped multilevel inverter is adopted in this paper. It is obtained from a configuration of 24 switching devices and 18 clamping diodes as shown in figure.

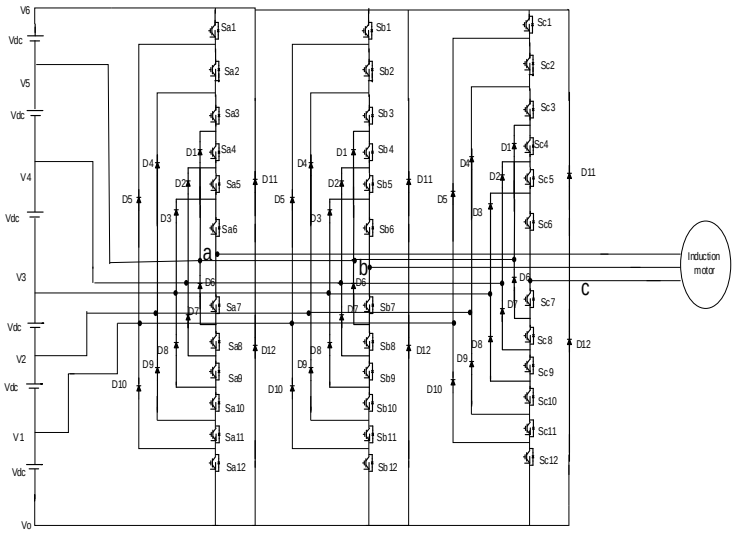

Figure 3. Diode-Clamped Multilevel Inverter Circuit Topologies for three phase seven-level fed induction motor

Table 3. Seven-level diode clamped switching sate for phase A

Vo	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Sa7	Sa8	Sa9	Sa10	Sa11	Sa12
Vdc/2	1	1	1	1	1	1	0	0	0	0	0	0
Vdc/3	0	1	1	1	1	1	1	0	0	0	0	0
Vdc/6	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	0
-Vdc/6	0	0	0	0	1	1	1	1	1	1	0	0
-Vdc/3	0	0	0	0	0	1	1	1	1	1	1	0
-Vdc/2	0	0	0	0	0	0	1	1	1	1	1	1

The sector is identified from three phase reference voltage and the corresponding voltage vector is selected from the switching table to generate the gating pulses for the inverter.

MODULATION TECHNIQUES

Pulse Width modulation (PWM) strategy is the developed issue to shift the total harmonic distortion (THD) of the present. it's usually recognized that increasing the switch frequency of the PWM pattern reduces the lower frequency harmonics by moving the switch frequency carrier harmonic and associated sideband harmonics any removed from the basic frequency element. The foremost advanced of these square measure Carrier primarily based are known as carrier based Pulse dimension Modulation (CB-PWM or SPWM). The operation principle of this methodology supported comparison of commanded voltage signal with the triangular carrier signal Result of this operation is rectangular signal. Width of the rectangle is proportional to average value of the commanded signal. signal of this operation is directly delivered to the semiconductor's driver, Carrier primarily based modulation for over 2 level converters needs a lot of carrier signals. For n-level convertor minimum n-1 carrier signals square measure required. Every carrier signal is to control the two switches. One switch is controlled directly by the pulse signal and second is controlled by negative sequence. Multiple carrier signals in structure converters creates varied prospects of mutual locations of these signals.
Typical possibilities for multi-carrier systems are:
• Phase Shifted Carriers (PSC)
• Level Shifted Carriers (LSC)

Phase Shifted Pulse Width Modulation Scheme (PSPWM)

Phase shifted PWM (PS-PWM) is used in Diode clamper Multilevel inverters, since each cell is modulated independently using sinusoidal unipolar PWM A carrier phase shift of 180^0/m for the CHB and of 360^0/m for the FC is introduced across the cells to generate the stepped multilevel output waveform with lower distortion (where m is the number of cells) the comparison of the ref and carrier by PSPWM as shown in Fig.4.

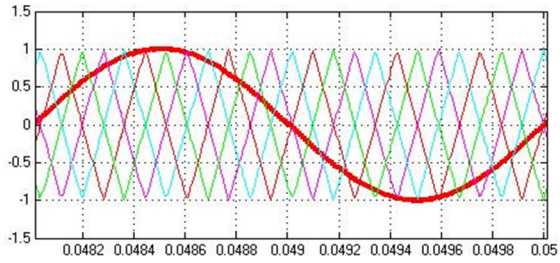

Figure 4. Phase shifted PWM Scheme

B. Level Shifted PWM Scheme (LSPWM)

Level shifted PWM (LS-PWM) is used for controlling voltage of a diode clamped multilevel inverter. The control principle of the level shifted SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For a three level inverter two carriers and for a five level inverter, four triangular carriers are needed. In general if an m-level inverter is employed, (m-1) carriers are needed. The carriers have the same frequency f_c and the same peak-to-peak amplitude A_C. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency f_m and amplitude A_m. At every instant, each carrier is compared with the modulating signal. Each comparison switches the switch "on" if the modulating signal is greater than the triangular carrier assigned to that switch.

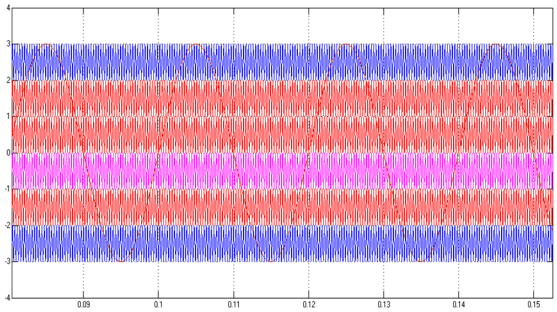

Figure 5. Level shifted PWM Scheme

MATLAB/SIMULATION RESULTS

Case 1: 3 level Diode Clamped Multi level Inverter fed Induction motor drive.

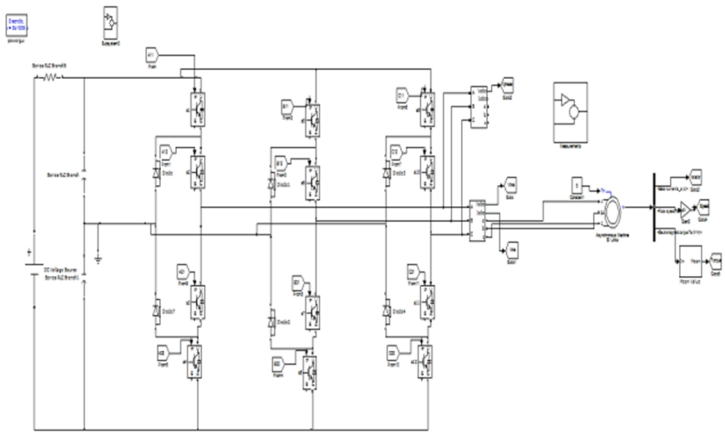

Figure 6. Simuilnk model of 3 level Diode Clamped Multi level Inverter fed Induction motor drive

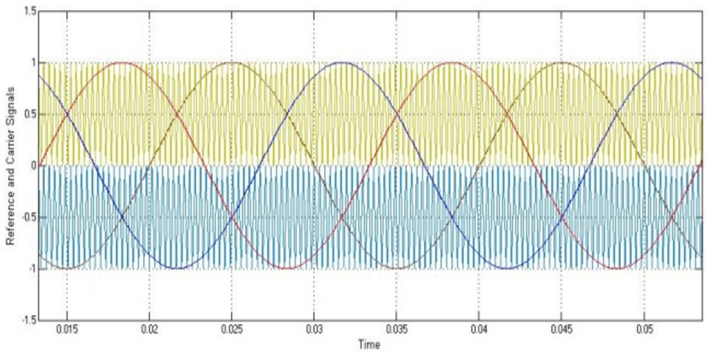

Figure 7. PWM technique for 3 level Diode Clamped Multi level inverter

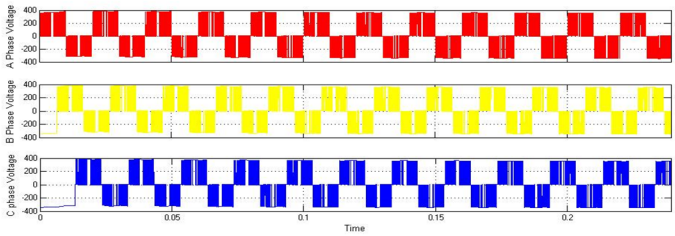

Figure 8. Simulated phase voltages output wave form of 3 level Diode Clamped Inverter

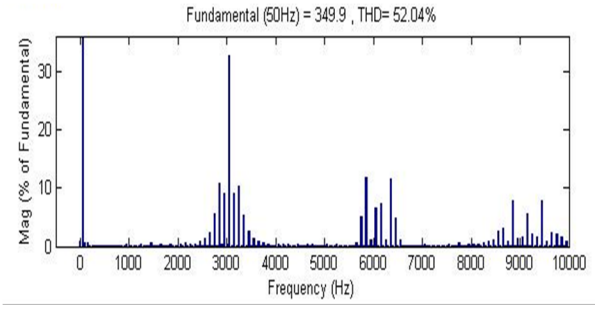

Figure 9. Total Harmonic Distortion of Phase voltage shows 52.04% at Modulation Index=1 for 3 level Diode Clamped Inverter

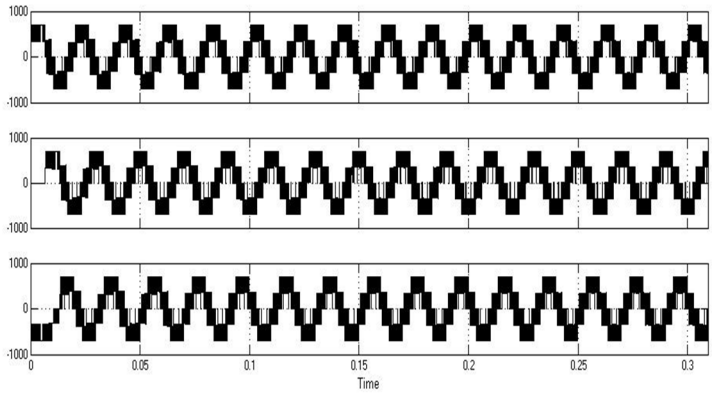

Figure 10. Simulated Line voltages output wave form of 3 level Diode Clamped Inverter

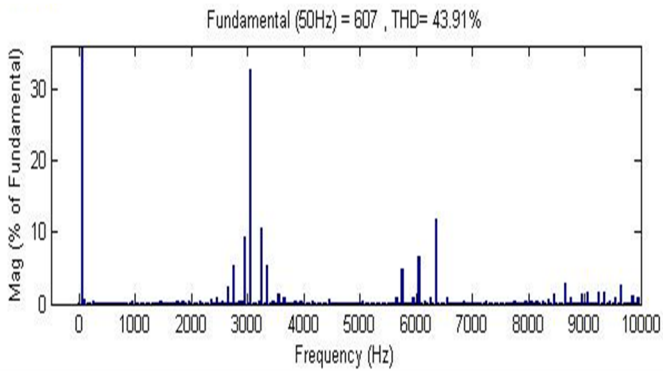

Figure 11. Total Harmonic Distortion of Line voltage shows 43.91% at Modulation Index=1 for 3 level Diode Clamped Inverter

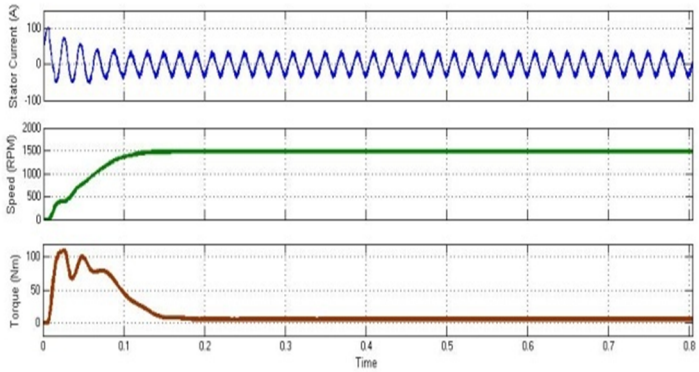

Figure 12. Simulated Current, Speed and torque characteristics wave forms of Induction motor under 3 level Diode Clamped Inverter

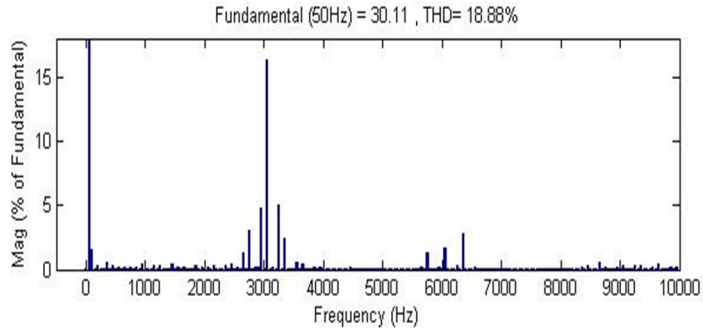

Figure 13. Total Harmonic Distortion of Stator Current shows 18.88% at Modulation Index=1 for 3 level Diode Clamped Inverter

Table 2

Total Harmonic Distortion for 3 Level Diode Clamped Multi level Inverter			
Modulation Index(MI)	Phase voltage	Line voltage	Stator current
0.3	184.90	156.69	31.06
0.5	125.66	117.64	32.16
0.7	86.34	90.87	38.08
0.9	64.29	57.62	24.43
1	52.04	43.91	18.88

Case 2: 5 level Diode Clamped Multi level Inverter fed Induction motor drive

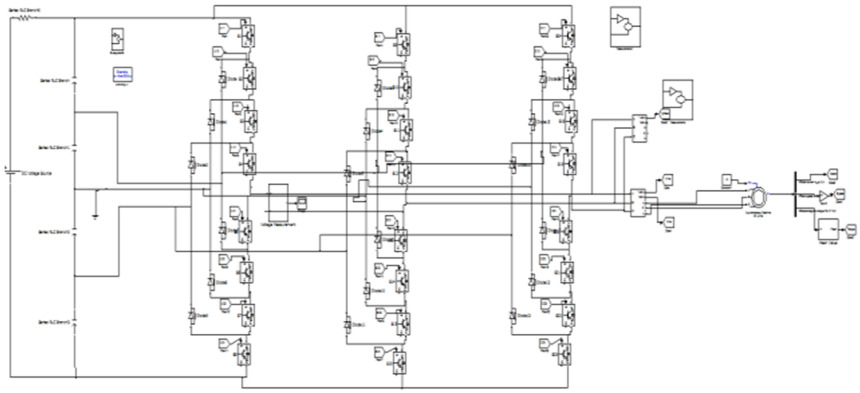

Figure 14. Simulink model of 5 level Diode Clamped Multi level Inverter fed Induction motor Drive

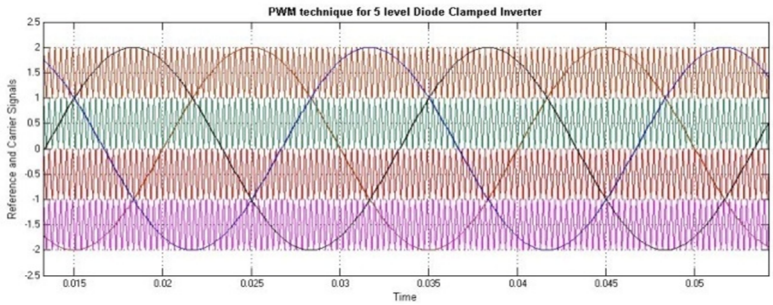

Figure 15. PWM technique for 5 level Diode Clamped Multi level inverter

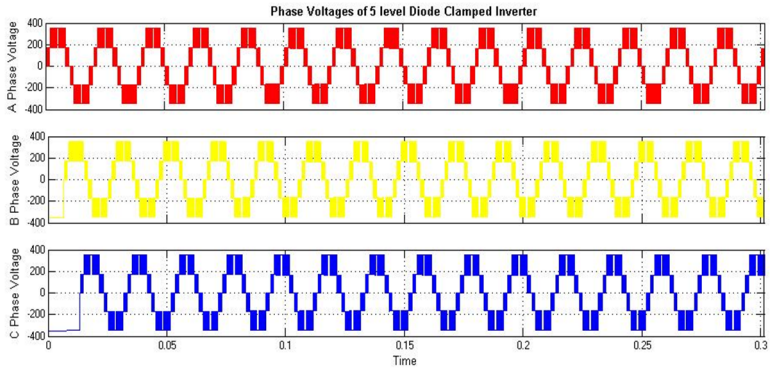

Figure 16. Simulated phase voltages output wave form of 5 level Diode Clamped Inverter

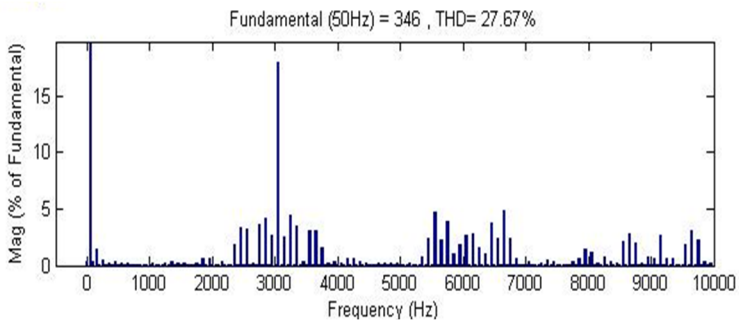

Figure 17. Total Harmonic Distortion of Phase voltage shows 27.67% at Modulation Index=1 for 5 level Diode Clamped Inverter

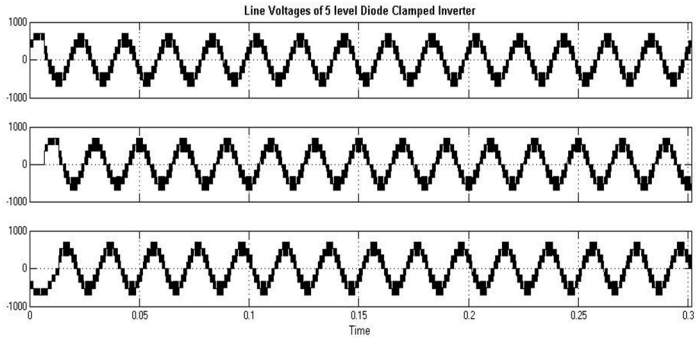

Figure 18. Simulated Line voltages output wave form of 5 level Diode Clamped Inverter

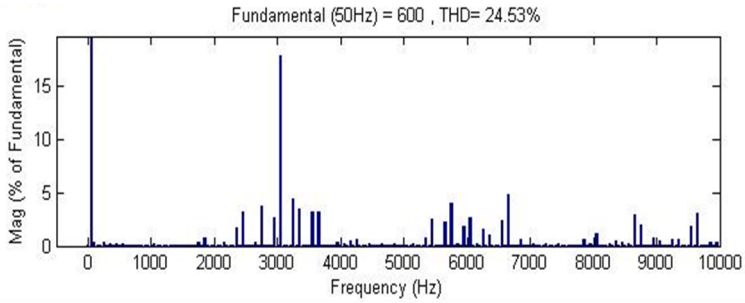

Figure 19. Total Harmonic Distortion of Line voltage shows 24.53% at Modulation Index=1 for 5 level Diode Clamped Inverter

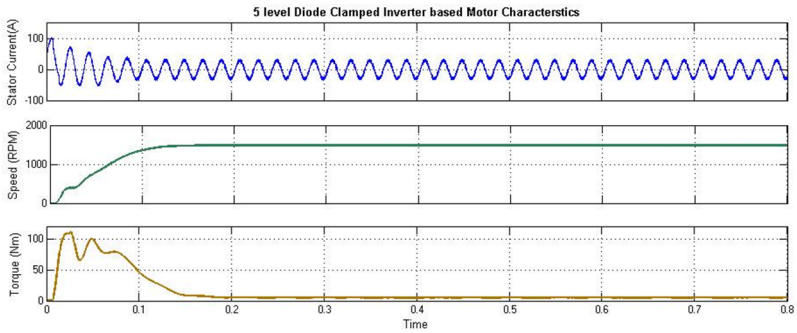

Figure 20. Simulated Current, Speed and torque characteristics wave forms of Induction motor under 5 level Diode Clamped Inverter

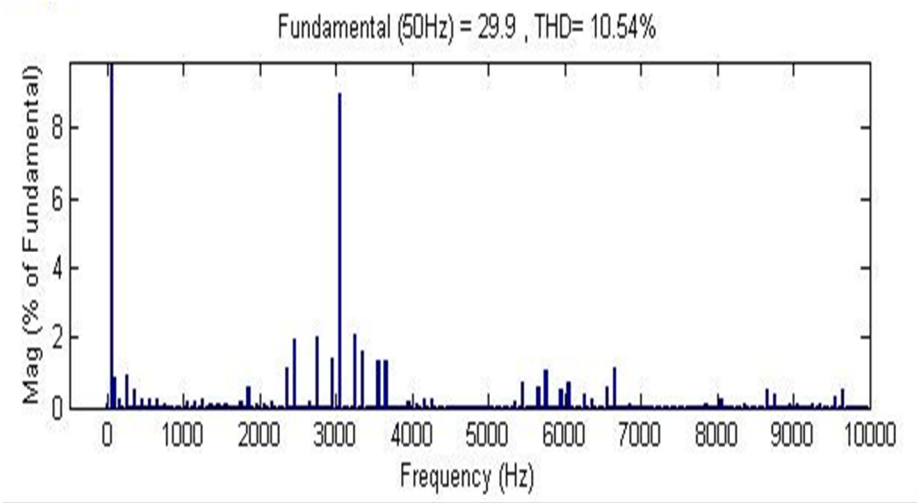

Figure 21. Total Harmonic Distortion of Stator Current shows 10.54% at Modulation Index=1 for 5 level Diode Clamped Inverter

Table 3

Total Harmonic Distortion for 5 Level Diode Clamped Multi level Inverter			
Modulation Index(MI)	Phase voltage	Line voltage	Stator current
0.3	106.94	100.87	20.42
0.5	52.84	44.51	10.79
0.7	46.39	41.50	17.24
0.9	35.37	32.8	14.16
1	27.67	24.53	10.54

Case 3: 7 level Diode Clamped Multi level Inverter fed Induction motor drive

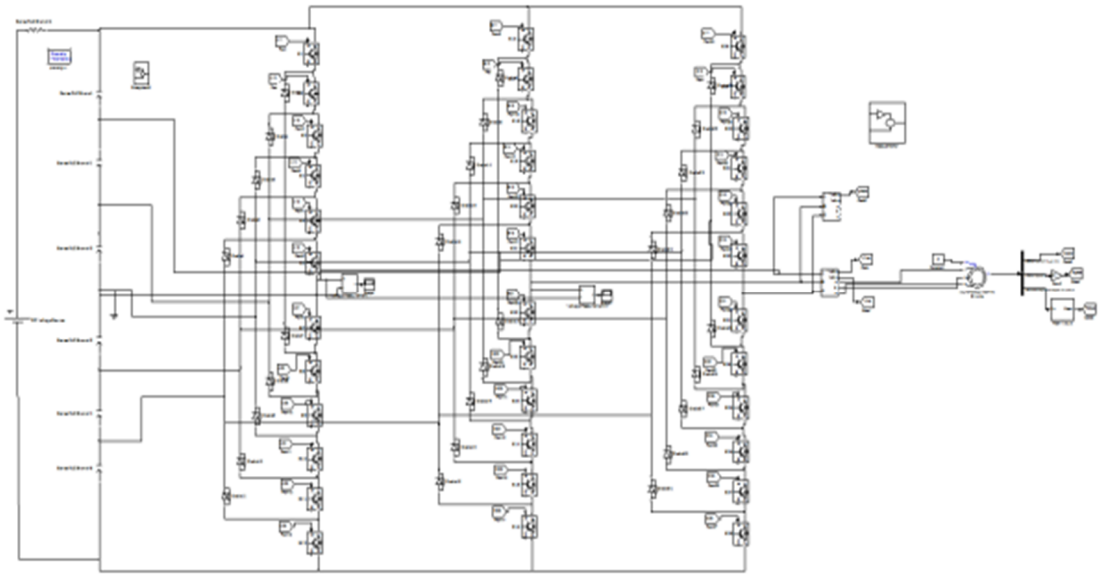

Figure 22. Simulated model of 7 level Diode Clamped Multi level Inverter fed Induction motor drive

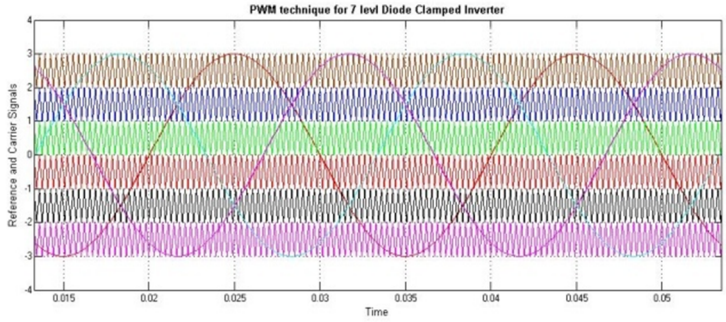

Figure 23. PWM technique for 7 level Diode Clamped Multi level inverter

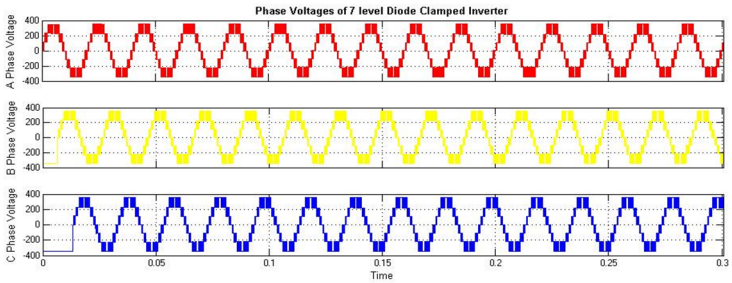

Figure 24. Simulated phase voltages output wave form of 7 level Diode Clamped Inverter

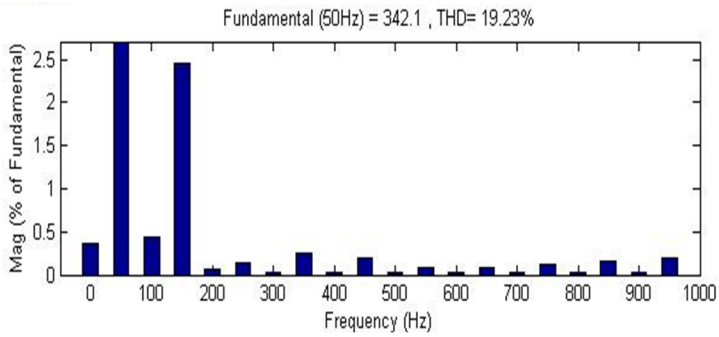

Figure 25. Total Harmonic Distortion of Phase voltage shows 19.23% at Modulation Index=1 for 7 level Diode Clamped Inverter

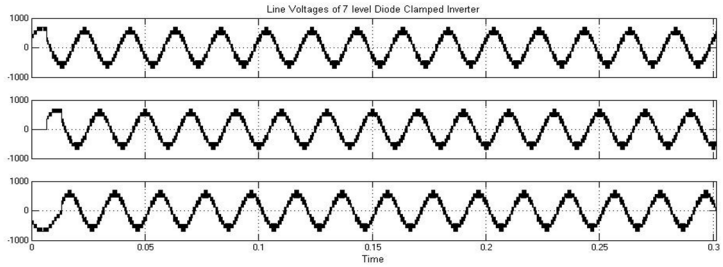

Figure 26. Simulated Line voltages output wave form of 7 level Diode Clamped Inverter

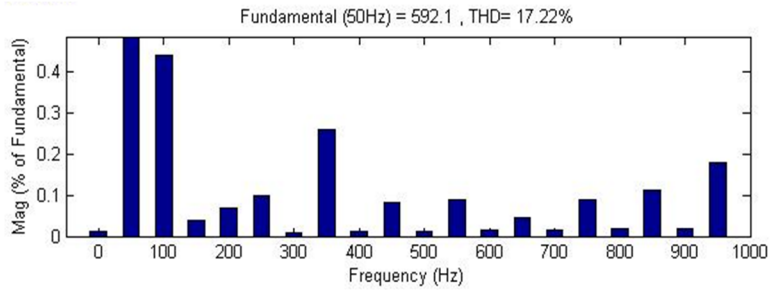

Figure 27. Total Harmonic Distortion of Line voltage shows 17.22% at Modulation Index=1 for 7 level Diode Clamped Inverter

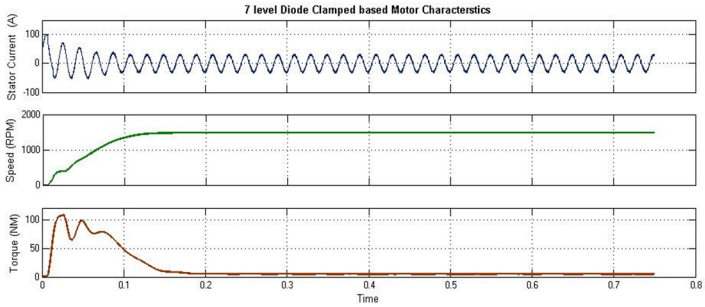

Figure 28. Simulated Current, Speed and torque characteristics wave forms of Induction motor under 7 level Diode Clamped Inverter

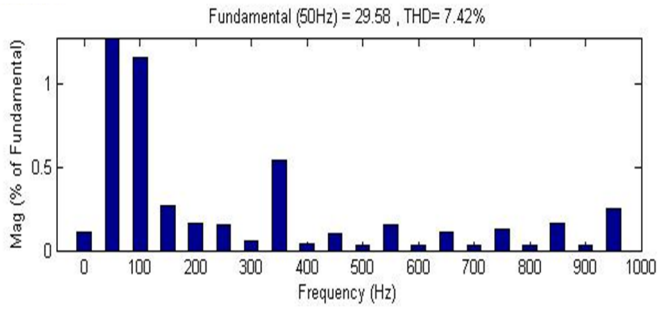

Figure 29. Total Harmonic Distortion of Stator Current shows 7.42% at Modulation Index=1 for 7 level Diode Clamped Inverter

Table 4

Total Harmonic Distortion for 7 Level Diode Clamped Multi level Inverter			
Modulation Index(MI)	Phase voltage	Line voltage	Stator current
0.3	65.34	58.46	11.21
0.5	46.92	42.40	10.44
0.7	27.66	23.64	9.06
0.9	25.37	23.04	10.24
1	19.23	17.22	7.42

CONCLUSION

In this paper, a Diode clamped based inverter with SPWM control algorithm for n-level Dc-Ac converter has been modelled and simulated with Matlab®/Simulink. This algorithmic rule will generate SPWM pulses for any level of inverter by ever-changing parameter n that is the number of electrical converter level. Simulation of three, 5, and 7 level inverter connected to induction motor has been performed and therefore the generated signals ThD is analysed. Simulation results provides a higher quality of stator coil current in terms of low harmonics, so reducing the adverse effects on of the machine life and eventually the electrical network which provides it. Base to ThD analyse for 0.3, 0.5, 0.7, 0.9 and 1 index of modulation, we've additionally highlighted that at seven-level, the harmonics is gradually

decreased. These latter will be simply eliminated with an easy low-pass filter. So it is not necessary to continue increasing the electrical converter level.

REFERENCES

F. Beaabjerg ,R. Teodorescu ,"*Multilevel converters - A survey*", Proc. EPE'99, pp. (1999).
M. Jia ,Z. Yan, "*An Integration SPWM Strategy for High-Frequency Link Matrix Converter With Adaptive Commutation in One Step Based on De-Re-Coupling Idea* ", Industrial Electronics, IEEE Transactions on, **Vol. 59 , pp. 116-128**, (2012).
J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "*Effect of PWM inverters on AC motor bearing currents and shaft voltages,*" IEEE Trans. Ind. Applicat., **vol. 32, pp. 250–259**, (Mar./Apr. 1996).
J.W. Dixon and B. T. Ooi, "*Dynamically stabilised indirect current controlled SPWM boost type 3-phase rectifier,*" in Conf. Rec. IEEE-IAS Annu. Meeting, (1988), **pp. 700–705**.
Y. Liang and C. O. Nwankpa, "*A New type of Statcom based on cascading voltage source inverters with phase-shifted unipolar SPWM,*" in Conf. Rec. IEEE-IAS Annu. Meeting, (1998), **pp. 1447–1453**.
L. Li, C. Dariusz, and Y. Liu, "*Multilevel space vector PWM technique based on phase-shift harmonic suppression*" Applied Power Electronics Conference and Exposition (APEC), **Vol.1, pp. 535-541**, (2000).
L. M. Tolbert, "*Multilevel Converters for Large Electric Drives*", IEEE Trans. on Ind. Application, **Vol. 35, pp. 36-44**, (1999).
L. Tian, S. Qiang, L. Wenhua, C. Yuanhua, and L. Jianguo, "*FPGAbased universal multilevel space vector modulator*" inProc. IECON 32nd Annu. Conf., **pp. 745–749**, (2005).
D. Ning-Yi, W. Man-Chung, and H. Ying-Duo, "*Application of a three level NPC inverter as a three-phase four-wire power 22 quality compensator by generalized 3DSVM*" IEEE Trans. Power Electron., **vol. 21, no. 2, pp. 440–449**, (Mar. 2006).
H. Le-Huy and L. A. Dessaint, "*An adaptive current control scheme for PWMsynchronous motor drives: Analysis and simulation,"* IEEE Trans. Power Electron., **vol. PE-4, no. 4, pp. 486–495**, (Oct. 1989).
M.-C. Wong, Z.-Y. Zhao, Y.-D. Han, and L.-B. Zhao, "*Three-Dimensional pulse-width modulation technique in three-level power inverters for three-phase four-wired system,"* IEEE Trans. Power Electron., **vol. 16, no. 3, pp. 418–427**, (May 2001).